DUAL SWITCHING REFERENCE VOLTAGES

FIELD OF THE INVENTION

[0001] This invention relates generally to electronic circuits and more particularly to methods and circuits for receiving digital electronic signals.

BACKGROUND OF THE INVENTION

[0002] Digital electronic signals are used to communicate digital information. This communication may be from on device to another, one integrated circuit (or chip) to another or within an integrated circuit itself. There has been a continuing need for this communication to be faster.

SUMMARY OF THE INVENTION

[0003] Two reference voltages and two differential receivers are used to detect low-to-high and high-to-low transitions on an input signal and set a received signal output. One reference voltage is set near but under the electrical high voltage level and the other is set near but above the electrical low voltage level. The reference voltage that is closest to the input signal is designated as the active reference voltage. When the input signal crosses the active reference voltage, the digital value of the

received signal output is changed. When the input signal then crosses the inactive reference voltage, the inactive reference voltage is made the active reference voltage. A dead-time is then waited where input signal crossings of the active reference voltage are ignored. After the dead-time, input signal crossings of the active reference voltage will change the received signal output.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is voltage vs. time plot of an exemplary input signal, dual reference voltages, and an example single reference voltage.

[0005] FIG. 2 is a flowchart illustrating steps to receive an input signal using dual reference voltages.

[0006] FIG. 3 is a schematic diagram illustrating a receiver circuit that utilizes dual reference voltages.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0007] FIG. 1 is voltage vs. time plot of an exemplary input signal **102**, dual reference voltages **106**, **108**, and an example single reference voltage **104**. The higher of the dual reference voltages **108** is labeled as V_{RH}. The lower of the dual reference voltages **106** is labeled as V_{RL}. The example single reference voltage is labeled V_1.

[0008] To illustrate the use of dual reference voltages **106**, **108**, examine FIG. 1 starting where input signal **102** goes from a dashed line to a solid line. At this point in time, V_{RH} is the active reference and V_{RL} is inactive. Also, this is during dead-time t_{DT} where the output is prevented from changing even though input signal **102** may cross the active reference voltage.

[0009] As shown in FIG. 1, some time after t_{DT}, input signal **102** transitions. This causes it to cross the active reference voltage, V_{RH}. Input signal **102** crossing the

active reference voltage results in the output switching state. If the input signal **102** being near V_{RH} is defined as being a logical "1", then input signal **102** crossing V_{RH} when it is the active reference voltage results in the output being switched from a logical 1 to a logical 0.

[0010] As input signal **102** continues its transition, it eventually crosses the inactive reference voltage, V_{RL}. At this point in time, V_{RL} is made the active reference voltage, V_{RH} is made the inactive reference voltage, and another dead-time, t_{DT}, begins. Once again, during the dead-time,t_{DT}, the output is prevented from changing even though input signal **102** may cross the now active reference voltage V_{RL}.

[0011] After the second dead-time, input signal **102** is shown transitioning from a low voltage level (below V_{RL}) to a high voltage level (above V_{RH}). This causes it to cross the active reference voltage, V_{RL}. Input signal **102** crossing the active reference voltage results in the output switching state. Since the state was a logical 0, the output is now switched to a logical 1. As input signal **102** completes this transition, it crosses the inactive reference voltage, V_{RH}. At this point in time, V_{RH} is made the active reference voltage, V_{RL} is made the inactive reference voltage, and another dead-time, t_{DT}, begins. Once again, during the dead-time, t_{DT}, the output is prevented from changing even though input signal **102** may cross the now active reference voltage V_{RH}.

[0012] In one embodiment, the dead-time, t_{DT}, is approximately one-half the minimum period of the input signal. However, depending upon the characteristics of the input signal, the dead-time could be chosen from a large range of times that include as little as 1/4 or less than the minimum period of the input signal to as large as the minimum period of the input signal.

[0013] To illustrate one of the advantages of dual switching reference voltages, note the time from input signal **102** crossing an active reference voltage to input signal **102** crossing the example single reference voltage. This is illustrated in one spot on FIG. 1 a Δt. Since the output is switched when the input signal **102** crosses the active reference voltage with the dual

switching reference voltages, and the output in an example single reference voltage only switches when the input voltage crosses the single reference voltage **104**, then the time represented by Δt illustrates how much faster the dual switching reference voltages can detect changes on the input signal **102**.

[0014] FIG. 2 is a flowchart illustrating steps to receive an input signal using dual reference voltages. In a step **202**, the receiving system has an active reference voltage and an inactive reference voltage as it waits until the input crosses the active reference voltage before proceeding to step **204**. In a step **204**, the output of the receiving system is changed to a logic state that is indicative of the input voltage being at or near the inactive reference voltage. For example, if a first reference voltage is the active reference voltage and the input being below that first reference voltage indicates a logical zero should be output by the receiving system and a second reference voltage is the inactive reference voltage and the input being above that second reference voltage indicates a logical one should be output by the receiving system, then when the input voltage crosses the first reference voltage, the receiving system should change its output from a logical zero to a logical one. After step **204**, the process continues to step **206**.

[0015] In a step **206**, the system waits for the input to cross the inactive reference voltage before proceeding to step **208**. In a step **208,** the system swaps the active and inactive reference voltages so that the previously active reference voltage is now the inactive reference voltage and the previously inactive reference voltage is now the active reference voltage. After step **208**, the process continues to step **210**. In a step **210**, the receiving system holds its output in its current state for a predetermined dead-time. During this dead-time, crossing of the active or inactive reference voltage are ignored and have no effect upon the state of the output or which reference voltage

is active and which is inactive. After the predetermined dead-time has expired, the process proceeds back to step **202**.

[0016] FIG. 3 is a schematic diagram illustrating a receiver circuit that utilizes dual reference voltages. In FIG. 3, input signal, IN, is connected to the non-inverting inputs of comparators **302** and **304**. A first reference voltage, V_{RL}, is connected to the inverting input of comparator **304**. A second reference voltage, V_{RH}, is connected to the inverting input of comparator **302**.

[0017] The output of comparator **302** is connected to a first input of NOR gate **314**, a first input of AND gate **312** and the "1" input of multiplexor (MUX) **306**. The output of comparator **304** is connected to a second input of NOR gate **314**, a second input of AND gate **312** and the "0" input of MUX **306**. The "1" input of MUX **306** is the input whose state is placed on the output of the MUX when the control input is a logical "1". Likewise, the "0" input of MUX **306** is the input whose state is placed on the output of the MUX when the control input is a logical "0".

[0018] The output of AND gate **312** is connected to the SET (S) input of RS flip-flop **316**. The output of NOR gate **314** is connected to the RESET (R) input of RS flip-flop **316**. Accordingly, when the output of AND gate **312** goes to a logical "1" the output of RS flip-flop **316**, Q, either stays, or is set to a logical "1". When the output of NOR gate **314** goes to a logical "1" the output of RS flip-flop **316**, Q, either stays, or is reset to a logical "0".

[0019] The output of RS flip-flop **316**, Q, is connected to the control input of MUX **306**, a first input of XNOR gate **322**, and the input of a delay element **320**. The output of delay element **320** is a copy of the signal on the input of the delay element **320** delayed by a predetermined time delay. This may be constructed from any number of circuits and devices well known in the art including a string of inverters.

The length of this predetermined time delay is a significant portion of the dead-time discussed above. The output of delay element **320** is connected to a second input of NOR gate **322**. The output of XNOR gate **322** is connected to the control terminal of pass-gate **310**. Pass-gate **310** is connected between the output of MUX **306** and the output of the receiver circuit, OUT, such that when control terminal of pass-gate **310** is a logical "1", the output of MUX **306** is connected to the output of the receiver circuit, OUT. Also connected to OUT is one node of two cross-coupled inverters **308**. These cross-coupled inverters act to hold the last value passed through pass-gate **310** when pass-gate **310** is not on (i.e. when the control terminal of pass gate **310** is a logical "0".)

[0020] To illustrate the functioning of the receiver circuit shown in FIG. 3, assume that the input signal, IN is lower than both the first and second reference voltages, V_{RL} and V_{RH}, that V_{RL} is the active reference voltage, that V_{RL} is lower than V_{RH}, and that the dead-time has expired. This would mean that the output of RS flip-flop **316** is a logical "0" (indicating that V_{RL} is the active reference voltage) and the output of XNOR **322** is a logical "1" (indicating that the dead-time has expired.) Since the output of RS flip-flop **316** is a logical "0", MUX **306** is outputting the value on its "0" input which is the output of comparator **304** (which is a logical "0"). The output of MUX **306** is also being passed to the output of the receiver, OUT, since the output of XNOR **322** is controlling pass-gate **310** to be on. The receiver will remain in this state until the input signal, IN, crosses the active reference voltage, V_{RL}.

[0021] When the input signal, IN, crosses the active reference voltage, V_{RL}, the output of comparator **304** changes from a logical "0" to a logical "1". This change passes through MUX **306**, pass-gate **310** to the output of the receiver, OUT. The

receiver will remain in this state until the input signal, IN, crosses the inactive reference voltage.

[0022] When the input signal, IN, crosses the inactive reference voltage, V_{RH}, the output of comparator **302** changes from a logical "0" to a logical "1". With the output of comparator **304** already at a logical "1", this change means both inputs to AND gate **312** are now logical "1's" so the output of AND gate **312** changes from a logical "0" to a logical "1". This sets the output of RS flip-flop, Q, to a logical "1". The change in the output of RS flip-flop **316** changes the input being selected by MUX **306** from its "0" input to its "1" input. This indicates that V_{RH} is now the active reference voltage and V_{RL} is now the inactive reference voltage.

[0023] The change in the output of RS flip-flop **316** also causes the output of XNOR gate **322** to go to a logical "0" for approximately the delay time of time delay **320**. While the output of XNOR gate **322** is at a logical "0", pass-gate **310** is off so changes on the output of comparator **302** as selected by MUX **306** won't be reflected on the output of the receiver. After approximately the delay time of time delay **320**, the output of XNOR gate **322** changes back to a logical "1" and changes on the output of comparator **302** due to the input voltage crossing the active reference voltage will be reflected on the receiver output, OUT. A similar process occurs as the input voltage falls crossing V_{RH} then V_{RL} with the output of the receiver changing to a logical "0" and then V_{RL} being made the active reference voltage.

[0024] Although several specific embodiments of the invention have been described and illustrated, the invention is no to be limited to the specific forms or arrangements of parts so described and illustrated. The invention is limited only by the claims.